CLAIMS:

1. A method of forming integrated circuit devices comprising:

forming a plurality of patterned device outlines over a semiconductive substrate;

forming electrically insulative spacers on at least a portion of the patterned device outlines; and

forming a plurality of substantially identically shaped devices relative to the patterned device outlines, at least two individual devices of the plurality being spaced from one another by a distance no greater than a width of an interposed electrically insulative spacer.

2. The method of forming integrated circuit devices of claim 1, wherein the devices are elongated electrically conductive lines.

3. The method of forming integrated circuit devices of claim 1, wherein the devices include capacitors of a DRAM array.

4. The method of forming integrated circuit devices of claim 1, wherein the plurality of devices are formed along a line, respective alternate devices along the line having a substantially common width dimension.

5. The method of forming integrated circuit devices of claim 1, wherein the plurality of devices are formed along a line, respective adjacent devices along the line having different width dimensions.

6. The method of forming integrated circuit devices of claim 1, wherein the devices include capacitors of a DRAM array, the capacitors being formed in rows, respective alternate capacitors in a row having substantially similar width profiles transverse the row.

7. The method of forming integrated circuit devices of claim 1, wherein the devices include capacitors of a DRAM array, the capacitors being formed in rows, adjacent capacitors in a row having different width profiles transverse the row.

8. The method of forming integrated circuit devices of claim 1, wherein the devices include capacitors of a DRAM array, the capacitors being formed in rows, respective alternate capacitors in a row having substantially similar width profiles transverse the row, adjacent capacitors in the row having different width profiles transverse the row.

9. A method of forming a plurality of integrated circuitry devices on a substrate comprising:

forming a plurality of spaced, upstanding, anisotropically etched electrically insulative spacers; and

forming a plurality of devices over the substrate intermediate the spacers with the spacers being positioned intermediate adjacent devices, adjacent devices having a pitch which is substantially no greater than about the distance between a pair of adjacent spacers plus the width of the spacer between the adjacent devices.

10. The method of forming a plurality of integrated circuitry devices of claim 9, wherein the devices are conductive lines.

11. The method of forming a plurality of integrated circuitry devices of claim 9, wherein the devices are capacitors.

12. The method of forming a plurality of integrated circuitry devices of claim 9, wherein the devices are capacitors of a DRAM device.

13. A DRAM capacitor forming method comprising the steps of:

forming a plurality of patterned outlines over a semiconductive substrate to define individual areas for a plurality of capacitors to be formed;

partitioning said individual areas from one another by a non-conducting partition; and

forming capacitors in at least some of the respective partitioned areas, the respective capacitors being separated from immediately adjacent capacitors by a distance substantially no greater than the width of the partition therebetween.

14. The DRAM capacitor forming method of claim 13, wherein the partitioning step comprises:

etching a first set of capacitor container openings, individual container openings having at least one upright sidewall; and

etching a second set of capacitor container openings adjacent respective first set container openings and separated therefrom by respective non-conducting partitions.

15. The DRAM capacitor forming method of claim 13, wherein the partitioning step comprises:

etching a first set of capacitor container openings, individual container openings having at least one upright sidewall;

forming insulative material over the substrate;

anisotropically etching the insulative material to provide partitions over at least some of the upright sidewalls; and

etching a second set of capacitor container openings immediately adjacent the provided partitions.

16. The DRAM capacitor forming method of claim 13 wherein individual defined areas, when viewed from a point above the substrate, approximate diamond shapes.

17. A DRAM capacitor forming method comprising the steps of:

forming a pair of adjacent capacitor containers over a substrate by etching a first capacitor container opening having at least one upright sidewall;

forming an electrically insulative spacer on the upright sidewall;

selectively etching a second capacitor container opening adjacent the formed spacer;

forming capacitors in the capacitor containers, adjacent capacitors having a separation distance therebetween which is substantially no greater than the width of the spacer between the adjacent capacitors.

18. The DRAM capacitor forming method of claim 17, wherein the step of forming the electrically insulative spacer comprises:

forming an insulative material over the substrate; and

anisotropically etching the insulative material to form the spacer.

19. The DRAM capacitor forming method of claim 17, wherein individual capacitor containers are generally triangularly shaped when viewed from a point above the substrate.

20. A method of forming capacitors comprising forming an array of capacitor pairs on a substrate, the array being defined in part by a plurality of lines, individual lines containing at least one pair of capacitors, individual capacitors of said at least one pair of capacitors being separated by substantially no more than an electrically insulative anisotropically etched spacer disposed therebetween.

21. The method of forming capacitors of claim 20 further comprising prior to forming the array of capacitor pairs, forming a plurality of bit line contacts in individual lines, individual capacitor pairs being bounded by at least two bit line contacts.

22. The method of forming capacitors of claim 20 wherein individual capacitor pairs have a pitch no greater than about a lateral width dimension of one of the capacitors plus the width of the anisotropically etched spacer between the capacitors of an individual pair.

23. A DRAM capacitor array comprising:

a substrate;

a first set of capacitors over the substrate; and

a second set of capacitors over the substrate, individual capacitors of the first set being bounded by at least three capacitors from the second set, individual first set capacitors having a closest separation distance from at least one of the three capacitors from the second set which is substantially no more than a width of an interposed electrically insulative anisotropically etched spacer.

24. The DRAM capacitor array of claim 23, wherein individual bounded first set capacitors have closest separation distances from no less than two of the three capacitors from the second set, said closest separation distances being substantially no more than a width of an interposed electrically insulative anisotropically etched spacer.

25. The DRAM capacitor array of claim 23 wherein individual bounded first set capacitors have closest separation distances from the three capacitors from the second set which are substantially no more than a width of an interposed electrically insulative anisotropically etched spacer.

26. A method of forming a plurality of capacitors in a semiconductor memory device comprising the steps of:

selectively removing substrate material to define a first set of containers;

forming sidewall spacers adjacent container sidewalls;

selectively removing remaining substrate material adjacent the spacers to define a second set of containers; and

forming capacitors in the containers separated only by the spacers.

27. The method of forming a plurality of capacitors of claim 26 further comprising prior to defining the first set of containers:

forming a plurality of bit line contact openings over the substrate, individual bit line contact openings having at least one sidewall; and

covering the at least one sidewall of the plurality of bit line contact openings with an insulating material.

28. The method of forming a plurality of capacitors of claim 26 further comprising prior to defining the first set of containers:

forming a plurality of bit line contact openings over the substrate, individual bit line contact openings having at least one sidewall;

covering the at least one sidewall of the plurality of bit line contact openings with an insulating material;

etching the insulating material to form sidewall spacers; and

forming electrically conductive material in the bit line contact openings to provide bit line contacts,

wherein the defining of the first set of containers includes selectively etching the first set of containers relative to the sidewall spacers and the electrically conductive material of the bit line contacts.

29. A DRAM capacitor forming method comprising forming a plurality of pairs of adjacent capacitors in respective adjacent capacitor containers separated by substantially no more than anisotropically etched sidewall spacers.

30. The DRAM capacitor forming method of claim 29, wherein individual pairs of adjacent capacitors, when viewed from a point over the substrate are approximately diamond shaped.

31. The DRAM capacitor forming method of claim 29 further comprising forming a plurality of bit line contact openings over the substrate prior to forming the capacitor pairs.

32. The DRAM capacitor forming method of claim 29 further comprising forming a plurality of bit line contact openings over the substrate prior to forming the capacitor pairs, and wherein individual pairs of adjacent capacitors, when viewed from a point over the substrate are approximately diamond shaped, individual bit line contact openings being positioned in respective corners of the diamonds.

33. A capacitor array for a DRAM comprising:

a plurality of bit line contacts to a substrate; and

a plurality of capacitor pairs selectively alternately etched over a substrate along etch axes which are generally orthogonal relative to the substrate, individual capacitor pairs having an area which, when viewed from outwardly of the substrate from a point on such etch axes, approximates a parallelogram which is bounded at a plurality of its corners by individual bit line contacts.

34. A processing method of forming a capacitor array for a DRAM comprising:

forming a plurality of bit line contacts to a substrate; and

forming a plurality of capacitor pairs, individual pairs being selectively alternately etched over a substrate and along etch axes which are generally orthogonal relative to the substrate, individual capacitor pairs having an area which, when viewed from outwardly of the substrate from a point on such etch axes, approximates a parallelogram which is bounded at a plurality of its corners by individual bit line contacts.

35. A method of forming a plurality of DRAM capacitors comprising:

etching capacitor container openings for an array in a substrate in at least two separate etching steps, and forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps.

36. The method of claim 35 wherein the forming electrically insulative partitions step comprises:

forming insulative material over the substrate; and

conducting an anisotropic etch of the insulative material to a degree sufficient to leave the partitions.

37. A processing method of forming a plurality of DRAM capacitors comprising etching capacitor container openings for a capacitor array in a substrate in two separate etching steps.

38. A DRAM capacitor array comprising:

a plurality of 6-capacitor geometries over a substrate, individual 6-capacitor geometries being defined by a plurality of individual generally polygonal capacitor geometries, and

further, individual 6-capacitor geometries, when viewed from above the substrate, approximating a hexagon, each individual side of which being defined by a side of a different respective one of the individual polygonal capacitor geometries.

39. The DRAM capacitor array of claim 38, wherein individual polygonal capacitor geometries, when viewed from above the substrate approximate a wedge shape.

40. The DRAM capacitor array of claim 38, wherein individual polygonal capacitor geometries, when viewed from above the substrate approximate a triangle.

41. The DRAM capacitor array of claim 38, wherein individual polygonal capacitor geometries, when viewed from above the substrate approximate an isosceles triangle.

42. The DRAM capacitor array of claim 38, wherein individual polygonal capacitor geometries, when viewed from above the substrate approximate an isosceles triangle equal adjacent angles of which approximate a range of between about 50° to 70°.

43. The DRAM capacitor array of claim 38, wherein individual polygonal capacitor geometries, when viewed from above the substrate approximate an isosceles triangle equal adjacent angles of which approximate about 65°.

44. The DRAM capacitor array of claim 38, wherein the hexagon can be bisected into halves containing exactly three individual polygonal capacitor geometries.

45. A DRAM capacitor array comprising:

a plurality of 3-capacitor geometries over a substrate, individual 3-capacitor geometries, when viewed from above the substrate being defined by a pair of overlapping approximated parallelograms, the intersection of which approximates a triangle.

46. A method of forming adjacent devices over a substrate comprising:

lithographically forming an array of patterned device outlines over a substrate, the outlines defining alternating male/female patterns;

forming electrically insulative sidewall spacers in the female patterns;

after forming the electrically insulative sidewall spacers, removing the male patterns; and

after removing the male patterns, forming circuit devices adjacent the spacers.

47. An integrated device array of substantially identically shaped devices comprising:

a plurality of spaced upstanding anisotropically etched electrically insulative spacers; and

a plurality of devices formed over the substrate intermediate the spacers with the spacers being positioned intermediate adjacent devices, adjacent devices having a pitch which is substantially no greater than about the distance between a pair of adjacent spacers plus the width of the spacer between the adjacent devices.

48. The integrated device array of claim 47, wherein the devices are conductive lines.

49. The integrated device array of claim 47, wherein the devices are capacitors.

50. The integrated device array of claim 47, wherein the devices are capacitors and the device array ~~forms~~ part of a DRAM device.

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